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[Document Name] Scope of Claim

[Claim 1]

A signal processing apparatus employing a second-order Volterra filter for an equalizer configured to equalize an input signal, characterized in that:

a quadratic filter for implementing a quadratic term of said second-order Volterra filter includes multiplication means for multiplying a first input signal with a second input signal; and

said multiplication means includes one or more delay means connected in series with one another for delaying a signal output from said multiplication means, each by unit time, coefficient multiplying means for multiplying a signal output from said multiplication means and a signal output from each of said delay means, each with a preset coefficient, and summation means for summing outputs of said coefficient multiplying means together.

[Claim 2]

The signal processing apparatus according to claim 1, characterized in that said quadratic filter includes a plurality of said multiplication means, one of said multiplication means employing a signal not delayed from said first signal, as said second signal, the remaining ones of said multiplication means each employing a signal delayed a preset time from said first signal, as said second signal.

[Claim 3]

The signal processing apparatus according to claim 1, characterized in that:

said quadratic filter includes n of said multiplication means, n being an integer not less than unity; and

a k' th one of said multiplication means, k being an integer such that $1 \leq k \leq n$, employing a signal corresponding to said first signal delayed by $(k-1)$ times of said unit time as said second

signal.

[Claim 4]

A signal processing method employing a second-order Volterra filter for equalizing an input signal, characterized in that processing equivalent to a quadratic term of said second-order Volterra filter includes

a multiplication step of multiplying a first signal with a second signal,

a delaying step of delaying a signal, output in said multiplication step, by one or more series-connected delay means, each by a unit time,

a coefficient multiplying step of multiplying a signal output in said multiplication step and a signal output from each of said delay means in said delaying step, each with a preset coefficient, and

a summing step of summing outputs of said coefficient multiplying step together.

[Claim 5]

A signal decoding apparatus employing a second-order Volterra filter as an equalizer for equalizing and decoding an input signal, comprising:

a linear filter for implementing a linear term of said second-order Volterra filter and for linear equalizing said input signal;

a quadratic filter for implementing a quadratic term of said second-order Volterra filter and for non-linear equalizing said input signal;

signal summing means for summing a signal output from said linear filter and a signal output from said quadratic filter together; and

most likelihood decoding means for most likelihood decoding

a signal output from said signal summing means,
the signal decoding apparatus being characterized in that
said quadratic filter includes multiplication means for
multiplying a first input signal and a second input signal together,
and

 said multiplication means includes one or more series-connected
 delaying means for delaying signals output from said multiplication
 means each by a preset unit time, coefficient multiplying means
 for multiplying a signal output from said multiplication means
 and a signal output from each of said delaying means, each with
 a preset coefficient, and summing means for summing outputs of
 said coefficient multiplying means together.

[Claim 6]

The signal decoding apparatus according to claim 5, characterized
in that said quadratic filter includes a plurality of said
multiplication means, one of said multiplication means employing
a signal not delayed from said first signal, as said second signal,
the remaining ones of said multiplication means each employing
a signal delayed a preset time from said first signal, as said
second signal.

[Claim 7]

The signal decoding apparatus according to claim 5, characterized
in that:

 said quadratic filter includes n of said multiplication means,
 n being an integer not less than unity; and

 a k'th one of said multiplication means, k being an integer
 such that $1 \leq k \leq n$, employing a signal corresponding to said first
 signal delayed by $(k-1)$ times of said unit time, as said second
 signal.

[Claim 8]

The signal decoding apparatus according to claim 5, further

comprising

error detection means for detecting an error between a signal at each discrete time output from said signal summing means and a target signal,

the signal decoding apparatus being characterized in that said coefficient multiplying means updates said preset coefficient every discrete time based on an error detected by said error detection means.

[Claim 9]

A signal decoding method employing a second-order Volterra filter in equalizing and decoding an input signal, comprising:

a linear filtering step of implementing processing equivalent to a linear term of said second-order Volterra filter and linear equalizing said input signal;

a quadratic filtering step of implementing processing equivalent to a quadratic term of said second-order Volterra filter and non-linear equalizing said input signal;

a signal summing step of summing a signal output in said linear filtering step and a signal output in said quadratic filtering step together; and

a most likelihood decoding step of most likelihood decoding a signal output in said signal summing step,

the signal decoding method being characterized in that said quadratic filtering step includes

a multiplication step of multiplying a first input signal with a second input signal,

a delaying step of delaying a signal, output by said multiplication step, by one or more series-connected delay means, each by a unit time,

a coefficient multiplying step of multiplying a signal output in said multiplication step and a signal output from each

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of said delay means in said delaying step, each with a preset coefficient, and

a summing step of summing outputs of said coefficient multiplying step together.

[Document Name] Specification

[Title of the Invention] SIGNAL PROCESSING APPARATUS AND METHOD
AND SIGNAL DECODING APPARATUS AND METHOD

[Technical Field]

[0001]

This invention relates to an apparatus and a method for signal processing for implementing a quadratic term of a second-order Volterra filter and for non-linear equalizing an input signal presenting non-linear distortion, and an apparatus and a method for decoding signals having such apparatus for signal processing.

[Background Art]

[0002]

Conventionally, a storage device exploiting a magnetic recording technique, an optical recording technique, or the like, or a signal processing apparatus employed in a wireless communication apparatus, as well as the software algorithm used therefor, has been designed on the basis of a linear signal processing theory based on the assumed linear performance of input signals. In general, these input signals are not formed only of perfectly linear signal components, and also contain non-linear components. However, these non-linear components are usually sufficiently low in power and therefore may be considered as approximately linear signals. For this reason, the signal processing apparatus based on the linearity theory has so far been used sufficiently efficaciously.

[0003]

However, with recent development in the storage technology and increase in the recording density, non-linear properties that are too large to be negligible have appeared in the reproduced signals. These non-linear properties account for deterioration in the performance of a Phase Locked Loop (PLL), in the convergence properties of an adaptive equalizing filter or in the ultimate

data error rate. Even though attempts have so far been made in increasing the recording density of a recording medium for further improving its recording capacity, non-linear signal distortion, caused by the use of a recording medium having a high recording density, or by the use of a detector exhibiting a high detection sensitivity but presenting a non-linear response to input or output signals, proves a significant factor that inhibits further performance improvement of the entire apparatus.

[0004]

Representative of the causes of these non-linear distortions of the reproduced signals are non-linear properties ascribable to the signal reproducing side and non-linear properties ascribable to the recording medium. As representative examples of the former type, there are a non-linear response and a base line shift of magnetic field-voltage transducing characteristics of an MR (Magneto Resistive) head, used as a reproducing head for magnetic recording, and also a non-linear response of a photodetector used for optical recording. On the other hand, as representative examples of the latter type, there are Non-Linear Inter-Symbol Interference (NLISI) under the state of high recording density of both the magnetic recording medium and the optical recording medium, vertical signal asymmetry, brought about by the non-linear performance of the reflectivity of the recording medium in the course of optical recording, and the like.

[0005]

The causes for ultimate deterioration in the error rate will now be scrutinized further.

In a linear adaptive equalizing filter that is mounted on a general signal processing apparatus and employs an LMS (Least Mean Square) algorithm or the like, convergence to tap coefficients, which will give the smallest square error value, is assured by

detecting an error signal between a target detection value conforming to a preset equalization system, represented by Partial Response (PR) or the like, and an actually detected signal, with respect to an input signal that is free of non-linear distortion. On the other hand, the non-linear distortion, represented by vertical asymmetry, cannot be corrected because of its theoretical structure.

[0006]

However, the linear adaptive equalizing filter searches, due to its algorithm structure, the tap coefficient which will simply minimize the square error obtained, and accordingly, in an input signal presenting vertical asymmetry, it is impossible to avoid the probability of convergence of the tap coefficients to values different from the ideal values that should converge so as to improve an ultimate data error rate as a normal target in a storage product.

This indicates the possibility of producing unforeseen new equalization errors (non-linear equalization errors), by following, in a case where an input signal to a linear adaptive equalizing filter has non-linear distortion, an adaptive equalizing algorithm in which correction of such non-linear equalization error is intrinsically not presupposed. Such non-linear equalization error leads to deterioration in the ultimate data error rate.

[0007]

In this consideration, such a technique implementing a polynominal filter as an adaptive equalization filter has been proposed as a method for non-linear equalization of a signal exhibiting non-linear distortion (for example, see Patent Documents 1 and 2). Researches into such polynominal filter, generally termed a Volterra filter, have so far been made in a variety of fields.

With the Volterra filter, it is possible to update and operate the tap coefficients in accordance with an adaptive equalization algorithm such as LMS or RLS (Recursive Least Square), and to perform

optimization in terms of the least square error. The theory of an adaptive equalization Volterra filter is described in detail in a document entitled "Adaptive Polynominal Filters" by V. John Matthews, IEEE SP Magazine, July 1991, pp.10 to 26.

[0008]

[Patent Document 1] Japanese Unexamined Patent Application Publication No. 2001-525101

[Patent Document 2] Japanese Patent Application Laid-open No. 2001-86585

[Disclosure of the Invention]

[Problems to be Solved by the Invention]

[0009]

Meanwhile, a customary second-order Volterra filter is represented by the following equation (1):

[0010]

[Equation 1]

$$y(k) = \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i_1=0}^{M_2-1} \sum_{i_2=0}^{M_2-1} h^{(2)}(i_1, i_2) \cdot x(k-i_1) \cdot x(k-i_2) \quad \dots (1)$$

where M_1 denotes a tap length of a linear filter, and M_2 denotes a tap length of a quadratic filter. In the equation (1), $y(k)$ denotes an output signal of the second-order Volterra filter at a given time point k , $x(k)$ denotes an input signal to the second-order Volterra filter at a given time point k , $h^{(1)}(i)$ denotes tap coefficients of the linear filter ($i = 0, 1, \dots, M_1-1$), and $h^{(2)}(i_1, i_2)$ denotes tap coefficients of the quadratic filter ($i_1 = 0, 1, \dots, M_2-1; i_2 = 0, 1, \dots, M_2-1$), respectively.

[0011]

Meanwhile, the second-order Volterra filter can be mounted

so that the number of taps thereof will sequentially be optimized in accordance with an adaptive equalization algorithm. In addition, if the optimum values of the tap coefficients of the linear and quadratic filters of the second-order Volterra filter are known in advance, the second-order Volterra filter may also be mounted as a filter of fixed tap coefficients.

[0012]

For completing calculations of the right side of the equation (1) by one cycle for the input signal $x(k)$, M_1 multiplication operations and $2 \times M_2 \times M_2$ multiplication operations are needed for the first and second terms of the right side, respectively. Moreover, the number of delay lines for holding the input signals $x(k)$ for the quadratic filter, corresponding to M_2 clocks, are also needed in addition to the input signal delay line to the linear filter.

[0013]

By exploiting known symmetry of the second-order Volterra filter, the tap coefficients of the quadratic filter satisfy the relationship indicated by the following equation (2):

[0014]

[Equation 2]

$$h^{(2)}(i_1, i_2) = h^{(2)}(i_2, i_1)$$

... (2).

[0015]

By exploiting the relationship of this equation (2), the above equation (1) may be simplified as the following equation (3).

[0016]

[Equation 3]

$$\begin{aligned}
 y(k) = & \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i=0}^{M_2-1} h^{(2)}(i,i) \cdot x^2(k-i) \\
 & + 2 \sum_{i_1=0}^{M_2-1} \sum_{i_2>i_1} h^{(2)}(i_1, i_2) \cdot x(k-i_1) \cdot x(k-i_2) \\
 & \dots (3) .
 \end{aligned}$$

[0017]

In this case, M_1 multiplication operations, $2 \times M_2$ multiplication operations, and $M_2 \times (M_2 - 1)$ multiplication operations are needed for the first, second and third terms of the right side of the equation (3), respectively.

[0018]

The results of comparison of the number of the multipliers of the quadratic filter of the second-order Volterra filter, indicated by the equations (1) and (3), for variable numbers M_2 , are shown in Fig.17 and in the following Table 1:

[0019]

[Table 1]

M2	Number of multipliers of quadratic term of equation (1)	Number of multipliers of quadratic term of equation (3)
1	2	2
2	8	6
3	18	12
4	32	20
5	50	30
6	72	42
7	98	56
8	128	72
9	162	90
10	200	110
11	242	132
12	288	156
13	338	182
14	392	210
15	450	240

[0020]

As may be seen from Fig.17 and Table 1, the larger the value of M_2 becomes, the more outstanding the effect of reducing the number of the multipliers by the equation (3) is. However, even with the configuration of the equation (3), as many as 240 multipliers are needed for the case of $M_2 = 15$.

[0021]

As described above, even though the higher order equalization Volterra filter is highly efficacious for equalizing an input signal

exhibiting non-linear distortion, many multiplication operations are needed if the filter is to be implemented by hardware or software, thus presenting implementation difficulties because of cost.

[0022]

The present invention has been proposed in view of such conventional circumstances, and an object of the present invention is to provide a signal processing apparatus and method capable of considerably reducing the number of multiplication operations in equalizing the input signal presenting non-linear distortion, and a signal decoding apparatus and method provided with such a signal processing apparatus.

[Means for Solving the Problems]

[0023]

In order to achieve the above-mentioned object, a signal processing apparatus according to the present invention employs a second-order Volterra filter for an equalizer configured to equalize an input signal. In the signal processing apparatus, a quadratic filter for implementing a quadratic term of the second-order Volterra filter includes multiplication means for multiplying a first input signal and a second input signal together, and the multiplication means includes one or more delay means connected in series with one another for delaying a signal output from the multiplication means, each by unit time, coefficient multiplying means for multiplying a signal output from the multiplication means and a signal output from each of the delay means, each with a preset coefficient, and summation means for summing outputs of the coefficient multiplying means together.

[0024]

Further, in order to achieve the above-mentioned object, a signal processing method according to the present invention employs a second-order Volterra filter for equalizing an input signal.

In the signal processing method, processing equivalent to a quadratic term of the second-order Volterra filter includes a multiplication step of multiplying a first signal with a second signal, a delaying step of delaying a signal, output in the multiplication step, by one or more series-connected delay means, each by a unit time, a coefficient multiplying step of multiplying a signal output in the multiplication step and a signal output from each of the delay means in the delaying step, with a preset coefficient, and a summing step of summing outputs of the coefficient multiplying step together.

[0025]

With the apparatus and method for signal processing, an input signal exhibiting non-linear distortion is equalized using the second-order Volterra filter. The multiplication processing, needed in the quadratic filter for implementing a quadratic term of the second-order Volterra filter, may be curtailed significantly.

[0026]

Further, in order to achieve the above-mentioned object, a signal decoding apparatus according to the present invention employs a second-order Volterra filter as an equalizer for equalizing and decoding an input signal. The signal decoding apparatus includes a linear filter for implementing a linear term of the second-order Volterra filter and for linear equalizing the input signal, a quadratic filter for implementing a quadratic term of the second-order Volterra filter and for non-linear equalizing the input signal, signal summing means for summing a signal output from the linear filter and a signal output from the quadratic filter, and most likelihood decoding means for most likelihood decoding a signal output from the signal summing means. The quadratic filter includes multiplication means for multiplying a first input signal with a second input signal. The multiplication means includes one or more series-connected delaying means for delaying signals

output from the multiplication means, each by a preset time, coefficient multiplying means for multiplying a signal output from the multiplication means and a signal output from each of the delaying means, each with a preset coefficient, and summing means for summing outputs of the coefficient multiplying means together.

[0027]

Further, in order to achieve the above-mentioned object, a signal decoding method according to the present invention employs a second-order Volterra filter in equalizing and decoding an input signal. The signal decoding method includes a linear filtering step of implementing processing equivalent to a linear term of the second-order Volterra filter and linear equalizing the input signal, a quadratic filtering step of implementing processing equivalent to a quadratic term of the second-order Volterra filter and non-linear equalizing the input signal, a signal summing step of summing a signal output in the linear filtering step and a signal output in the quadratic filtering step together, and a most likelihood decoding step of most likelihood decoding a signal output in the signal summing step. The quadratic filtering step includes a multiplication step of multiplying the first input signal with the second input signal, a delaying step of delaying a signal, output in the multiplication step, by one or more series-connected delay means, each by a unit time, a coefficient multiplying step of multiplying a signal output in the multiplication step and a signal output from each of the delay means in the delaying step, each with a preset coefficient, and a summing step of summing outputs of the coefficient multiplying step together.

[0028]

The apparatus and the method for signal decoding equalize and decode an input signal by the second-order Volterra filter, and include, in addition to a linear filter that implements the

linear term of the second-order Volterra filter, a quadratic filter that implements the quadratic term of the second-order Volterra filter and that significantly curtails the multiplication operations.

[Effect of the Invention]

[0029]

With the signal processing apparatus and method according to the present invention, the multiplication operations needed in equalizing the input signal by the quadratic filter of the second-order Volterra filter, the quadratic filter implementing the quadratic term of the second-order Volterra filter, may be reduced considerably, thus enabling the reduction in the circuit scale in implementing the quadratic filter using an LSI (Large-Scale Integrated Circuit), and also enabling the reduction in the processing volume in implementing the quadratic filter using a DSP (Digital Signal Processor) and software.

[0030]

With the signal decoding apparatus and method according to the present invention, there is provided the quadratic filter that implements the quadratic term of the second-order Volterra filter and that significantly reduce the multiplication operations in equalizing and decoding the input signal by the second-order Volterra filter, in addition to the linear section implementing the linear term of the second-order Volterra filter, thus effectively correcting the non-linear distortion by a smaller volume of multiplication operations.

[Best Mode for Carrying out the Invention]

[0031]

A technique employing a Volterra filter for non-linear equalization of a signal exhibiting non-linear distortion has been so far proposed.

[0032]

Here, with a tap length of a linear filter M_1 and with a tap length of a quadratic filter M_2 , a general second-order Volterra filter is represented by the following equation (4):

[0033]

[Equation 4]

$$y(k) = \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i_1=0}^{M_2-1} \sum_{i_2=0}^{M_2-1} h^{(2)}(i_1, i_2) \cdot x(k-i_1) \cdot x(k-i_2) \quad \dots (4)$$

where $y(k)$ is an output signal of the second-order Volterra filter at a given time point k , $x(k)$ is an input signal to the second-order Volterra filter at a given time point k , $h^{(1)}(i)$ is a tap coefficient of the linear filter ($i = 0, 1, \dots, M_1-1$), and $h^{(2)}(i_1, i_2)$ is a tap coefficient of the quadratic filter ($i_1 = 0, 1, \dots, M_2-1$; $i_2 = 0, 1, \dots, M_2-1$), respectively.

[0034]

For completing calculations of the right side of the equation (4) by one cycle for the input signal $x(k)$, M_1 times of multiplication operations and $2 \times M_2 \times M_2$ times of multiplication operations are needed for the first and quadratic terms of the right side, respectively. Moreover, the number of delay lines equivalent to M_2 clocks are needed, the delay lines holding the input signal $x(k)$ to the quadratic filter, in addition to the input signal delay line to the linear filter.

[0035]

It is also known that, by exploiting known symmetry of the second-order Volterra filter, the aforementioned equation (4) can be simplified as indicated by the following equation (5):

[0036]

[Equation 5]

$$\begin{aligned}
 y(k) = & \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i=0}^{M_2-1} h^{(2)}(i, i) \cdot x^2(k-i) \\
 & + 2 \sum_{i_1=0}^{M_2-1} \sum_{i_2 > i_1} h^{(2)}(i_1, i_2) \cdot x(k-i_1) \cdot x(k-i_2) \\
 & \dots (5).
 \end{aligned}$$

[0037]

In this case, M_1 times of multiplication operations, $2 \times M_2$ times of multiplication operations and $M_2 \times (M_2-1)$ times of multiplication operations are needed for the first, second and third terms of the right side of the equation (5), respectively.

[0038]

However, notwithstanding the simplification as in the equation (5), voluminous multiplication operations are needed for the quadratic filter if M_2 is of a large value. Hence, the second-order Volterra filter is difficult to be implemented in consideration of costs.

[0039]

Thus, in this embodiment, calculations for the quadratic filter of the second-order Volterra filter are simplified as described below, thereby reducing the volume of necessary multiplication operations considerably.

[0040]

Meanwhile, the signal processing apparatus of this embodiment non-linear equalizes an input signal exhibiting non-linear distortion by carrying out the calculations for the quadratic filter of the second-order Volterra filter. The signal decoding apparatus of this embodiment includes the above signal processing apparatus as a non-linear adaptive equalizing filter, in addition to an

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equalizing filter adapted to carry out calculations for the linear filter of the second-order Volterra filter, and equalizes and decodes signals recorded on the optical disc.

[0041]

In the following explanation, the technique of simplifying the calculations for the quadratic filter of the second-order Volterra filter is first explained. The configuration and the operation of a signal processing apparatus in this embodiment carrying out the simplified calculations are explained next.

[0042]

For simplifying the calculations of the quadratic filter, the quadratic term of the input signal of the second-order Volterra filter is first substituted as in the following equation (6):

[0043]

[Equation 6]

$$x(k - i_1) \cdot x(k - i_2) = x^{(2)}(k, i_1, i_2)$$

... (6).

[0044]

From this equation (6), the relationship of the following equations (7) and (8):

[0045]

[Equation 7]

$$x^{(2)}(k, i_1, i_2) = x^{(2)}(k, i_2, i_1)$$

... (7)

$$x^{(2)}(k, i_1 + m, i_2 + m) = x(k - m - i_1) \cdot x(k - m - i_2)$$
$$= x^{(2)}(k - m, i_1, i_2)$$

... (8)

may be derived readily.

[0046]

Moreover, using the equation (6), the above equation (4) may be rewritten as in the following equation (9):

[0047]

[Equation 8]

$$y(k) = \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i_1=0}^{M_2-1} \sum_{i_2=0}^{M_2-1} h^{(2)}(i_1, i_2) \cdot x^{(2)}(k, i_1, i_2) \dots (9).$$

[0048]

The quadratic term of the equation (9) may be deemed to be a sum of multiplication outputs obtained by multiplication of corresponding elements (i_1, i_2) of respective elements of a two-dimensional array $h^{(2)}(i_1, i_2)$ of quadratic tap coefficients having $M_2 \times M_2$ of elements, with respective elements of a two-dimensional array $x^{(2)}(k, i_1, i_2)$ of second-order signals, at a given time point k , having $M_2 \times M_2$ of elements.

[0049]

Hereinafter, a case of $M_2 = 6$ will be described as an example. Fig.1 is a conceptual diagram of a two-dimensional array $x^{(2)}(k, i_1, i_2)$ of the second-order signals having 6×6 elements. Further, Fig.2 is a conceptual diagram of a two-dimensional array $h^{(2)}(i_1, i_2)$ of second-order tap coefficients having 6×6 elements. The tap coefficients $h^{(2)}(i_1, i_2)$ of the second-order filter may be fixed, or may be sequentially updated by any adaptive equalization algorithm.

The second term of the aforementioned equation (9) is obtained by multiplying the corresponding elements (i_1, i_2) of Figs.1 and 2 with one another and by summing together the obtained terms.

[0050]

Here, using the equation (6), the aforementioned equation (5) may be rewritten as shown by the following equation (10):

[0051]

[Equation 9]

$$\begin{aligned}
 y(k) = & \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i=0}^{M_2-1} h^{(2)}(i, i) \cdot x^{(2)}(k, i, i) \\
 & + 2 \sum_{i_1=0}^{M_2-1} \sum_{i_2 > i_1} h^{(2)}(i_1, i_2) \cdot x^{(2)}(k, i_1, i_2) \\
 & \cdots (10).
 \end{aligned}$$

[0052]

Fig.3 shows in which portions of the two-dimensional array of Fig.1 are located the respective elements of the diagonal term $x^{(2)}(k, i, i)$ of the second-order signals contained in the quadratic term of the right side of the equation (10). As may be seen from Fig.3, the respective elements of the diagonal term $x^{(2)}(k, i, i)$ are elements in the two-dimensional array with $i_1 = i_2$, that is, diagonal elements. In similar manner, Fig.4 shows in which portions of the two-dimensional array of Fig.1 are located the respective elements of non-diagonal terms $x^{(2)}(k, i_1, i_2)$ contained in the third term of the right side of the equation (10). As may be seen from Fig.4, the respective elements of the non-diagonal terms $x^{(2)}(k, i_1, i_2)$ are elements in the two-dimensional array with $i_1 < i_2$, that is, elements of an upper triangle excluding the diagonal elements.

[0053]

A two-dimensional array $W^{(2)}(k, i_1, i_2)$ having 6×6 elements at a given time point k is defined as in the following equation (11):

[0054]

[Equation 10]

$$W^{(2)}(k, i_1, i_2) = \begin{cases} x^{(2)}(k, i_1, i_2), & i_1 = i_2, \\ 2x^{(2)}(k, i_1, i_2), & i_1 < i_2, \\ 0, & \text{else.} \end{cases} \quad \dots (11).$$

[0055]

In this case, for $W^{(2)}(k, i_1, i_2)$, the relationship of the following equation (12) :

[0056]

[Equation 11]

$$W^{(2)}(k, i_1 + m, i_2 + m) = W^{(2)}(k - m, i_1, i_2) \quad \dots (12)$$

may readily be derived from the equation (8), for an optional integer m .

[0057]

Moreover, using the equation (11), the aforementioned equation (10) may be expressed by the following equation (13). The equation (14) expresses the equation (13) by the sum of the output of the linear filter shown by the equation (15) and the output of the quadratic filter shown by the equation (16).

[0058]

[Equation 12]

$$y(k) = \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) + \sum_{i_1=0}^{M_2-1} \sum_{i_2 \geq i_1}^{M_2-1} h^{(2)}(i_1, i_2) \cdot W^{(2)}x(k, i_1, i_2) \quad \dots (13)$$

$$y(k) = y^{(1)}(k) + y^{(2)}(k)$$

... (14)

$$y^{(1)}(k) = \sum_{i=0}^{M_1-1} h^{(1)}(i) \cdot x(k-i) \quad \dots (15)$$

$$y^{(2)}(k) = \sum_{i_1=0}^{M_2-1} \sum_{i_2 \geq i_1}^{M_2-1} h^{(2)}(i_1, i_2) \cdot W^{(2)} x(k, i_1, i_2) \quad \dots (16).$$

[0059]

Fig.5 shows respective elements of a two-dimensional array $W^{(2)}(k, i_1, i_2)$ contained in the term of the quadratic filter of the equation (13). As shown in Fig.5, $W^{(2)}(k, i_1, i_2)$ has zero values for components of a lower triangle excluding its diagonal elements.

Fig.6 shows, for comparison sake, a two-dimensional array in which the respective elements of Fig.5 are represented using $x^{(2)}(k, i_1, i_2)$ as in the equation (11).

[0060]

Fig.7 shows a two-dimensional array obtained by converting respective elements of Fig.5 using the equation (12). In this figure, $W^{(2)}(k-m, i_1, i_2)$ represents a signal obtained by delaying $W^{(2)}(k, i_1, i_2)$ by m clocks. For comparison, Fig.8 shows a two-dimensional array obtained by expressing the respective elements of Fig.7, using $x^{(2)}(k, i_1, i_2)$, as shown in the equation (11).

[0061]

In this case, the diagonal elements in Fig.7 are $W^{(2)}(k, 0, 0)$, $W^{(2)}(k-1, 0, 0)$, \dots , $W^{(2)}(k-5, 0, 0)$, which are equivalent to one-clock delayed versions of $W^{(2)}(k, 0, 0)$. Similarly, the elements parallel and neighboring to the diagonal elements are $W^{(2)}(k, 0, 1)$, $W^{(2)}(k-1, 0, 1)$, \dots , $W^{(2)}(k-4, 0, 1)$, which are equivalent to one-clock delayed versions of $W^{(2)}(k, 0, 1)$. That is, in Fig.7, the diagonal elements and the non-diagonal elements, which may be deemed to be multiple one-dimensional arrays parallel

to the diagonal elements, may be deemed to be outputs of the respective delay circuits in an FIR (Finite Impulse Response) filter. Moreover, the outputs of the respective delay elements form a quadratic filter by taking products of these outputs with second-order tap coefficients $h^{(2)}(i_1, i_2)$ having corresponding indexes (i_1, i_2) in the equations (12) and (13), and hence the portion of the quadratic filter forming the diagonal elements of Fig.7 and the portion of the quadratic filter formed by the non-diagonal elements parallel to the diagonal elements may be deemed to form respective independent FIR filters.

[0062]

Fig.9 shows an instance of a circuit configuration of a signal processing apparatus which, in consideration of the aforementioned equations (6) and (11), outputs $W^{(2)}(k, i_1, i_2)$ in the equation (13) when an input at a time point k is $x(k)$. Referring to Fig.9, the signal processing apparatus 10 is one in which six FIR filters (FIR0 to FIR5) are connected in parallel, each of which includes a multiplier and a delay circuit. A delay circuit is provided between the FIR filters. Out of these filters, the first FIR filter, indicated by FIR0 in Fig.9, outputs $W^{(2)}(k, 0, 0)$, $W^{(2)}(k-1, 0, 0)$, \dots , $W^{(2)}(k-5, 0, 0)$, which are the diagonal elements in Fig.7, whilst the second FIR filter, indicated by FIR1 in Fig.9, outputs $W^{(2)}(k, 0, 1)$, $W^{(2)}(k-1, 0, 1)$, \dots , $W^{(2)}(k-5, 0, 1)$, which are the elements parallel and neighboring to the diagonal elements, and so forth.

[0063]

In Fig.9, input signals $x(k)$ at a time point k are multiplied with each other by a multiplier 12₁ to output $W^{(2)}(k, 0, 0)$ ($= x(k) \cdot x(k)$). Simultaneously, $W^{(2)}(k-1, 0, 0)$, \dots , $W^{(2)}(k-5, 0, 0)$, which are signals delayed from the output signal by one clock each by delay circuits 14₁, 15₁, 16₁, 17₁ and 18₁, respectively, are output

from the delay circuits 14_1 , 15_1 , 16_1 , 17_1 and 18_1 , respectively.

The output from the multiplier 12_1 and the outputs from the delay circuits 14_1 , 15_1 , 16_1 , 17_1 and 18_1 are multiplied by multipliers 19_1 , 20_1 , 21_1 , 22_1 , 23_1 and 24_1 with corresponding tap coefficients $h^{(2)}(0, 0)$, $h^{(2)}(1, 1)$, $h^{(2)}(2, 2)$, $h^{(2)}(3, 3)$, $h^{(2)}(4, 4)$ and $h^{(2)}(5, 5)$, and the resulting outputs are summed together by an adder 25_1 to give an output of the filter FIR0.

[0064]

A multiplier 12_2 multiplies the input signal $x(k)$ at a time point k with the signal $x(k-1)$, one clock before, delayed by a delay circuit 11_2 . A multiplier 13_2 multiplies the resulting product with 2 to output $W^{(2)}(k, 0, 1)$ ($=2x(k) \cdot x(k-1)$). Simultaneously, $W^{(2)}(k-1, 0, 1)$, \dots , $W^{(2)}(k-4, 0, 1)$, which are signals delayed each by one clock by the delay circuits 14_2 , 15_2 , 16_2 and 17_2 , respectively, are output from the delay circuits 14_2 , 15_2 , 16_2 and 17_2 , respectively. The output from the multiplier 12_2 and the outputs from the delay circuits 14_2 , 15_2 , 16_2 and 17_2 are multiplied by multipliers 19_2 , 20_2 , 21_2 , 22_2 and 23_2 with corresponding tap coefficients $h^{(2)}(0, 1)$, $h^{(2)}(1, 2)$, $h^{(2)}(2, 3)$, $h^{(2)}(3, 4)$ and $h^{(2)}(4, 5)$, and the resulting outputs are summed together by an adder 25_2 to give an output of the filter FIR1.

[0065]

A multiplier 12_3 multiplies the input signal $x(k)$ at a time point k with the signal $x(k-2)$, two clocks before, delayed further by one clock by a delay circuit 11_3 . A multiplier 13_3 multiplies the resulting product with 2 to output $W^{(2)}(k, 0, 2)$ ($=2x(k) \cdot x(k-2)$). Simultaneously, $W^{(2)}(k-1, 0, 2)$, \dots , $W^{(2)}(k-3, 0, 2)$, which are signals delayed each by one clock by the delay circuits 14_3 , 15_3 and 16_3 , respectively, are output from the delay circuits 14_3 , 15_3 and 16_3 , respectively. The output from the multiplier 12_3 and the outputs from the delay circuits 14_3 , 15_3 and 16_3 are multiplied

by multipliers 19₃, 20₃, 21₃ and 22₃ with corresponding tap coefficients $h^{(2)}(0, 2)$, $h^{(2)}(1, 3)$, $h^{(2)}(2, 4)$ and $h^{(2)}(3, 5)$ and the resulting outputs are summed together by an adder 25₃ to give an output of the filter FIR2.

[0066]

A multiplier 12₄ multiplies the input signal $x(k)$ at a time point k with the signal $x(k-3)$, three clocks before, delayed further by one clock by a delay circuit 11₄. A multiplier 13₄ multiplies the resulting product with 2 to output $W^{(2)}(k, 0, 3)$ ($=2x(k) \cdot x(k-3)$). Simultaneously, $W^{(2)}(k-1, 0, 3)$ and $W^{(2)}(k-2, 0, 3)$, which are signals delayed each by one clock by the delay circuits 14₄ and 15₄, respectively, are output from the delay circuits 14₄ and 15₄, respectively. The output from the multiplier 12₄ and the outputs from the delay circuits 14₄ and 15₄ are multiplied by multipliers 19₄, 20₄ and 21₄, respectively, with corresponding tap coefficients $h^{(2)}(0, 3)$, $h^{(2)}(1, 4)$ and $h^{(2)}(2, 5)$, respectively, and the resulting outputs are summed together by an adder 25₄ to give an output of the filter FIR3.

[0067]

A multiplier 12₅ multiplies the input signal $x(k)$ at a time point k with the signal $x(k-4)$, four clocks before, delayed further by one clock by a delay circuit 11₅. A multiplier 13₅ multiplies the resulting product with 2 to output $W^{(2)}(k, 0, 4)$ ($=2x(k) \cdot x(k-4)$). Simultaneously, $W^{(2)}(k-1, 0, 4)$, which is a signal delayed by one clock by the delay circuit 14₅, is output from the delay circuit 14₅. The output from the multiplier 12₅ and the output from the delay circuit 14₅ are multiplied by multipliers 19₅ and 20₅, respectively, with corresponding tap coefficients $h^{(2)}(0, 4)$ and $h^{(2)}(1, 5)$, respectively, and the resulting outputs are summed together by an adder 25₅ to give an output of the filter FIR4.

[0068]

A multiplier 12_6 multiplies the input signal $x(k)$ at a time point k with the signal $x(k-5)$, five clocks before, delayed further by one clock by a delay circuit 11_6 . A multiplier 13_6 multiplies the resulting product with 2 to output $W^{(2)}(k, 0, 5)$ ($=2x(k) \cdot x(k-5)$). In addition, a multiplier 20_6 multiplies the output signal with a corresponding tap coefficient $h^{(2)}(0, 5)$, by a multiplier 19_6 , an output of which becomes an output of the FIR 5.

[0069]

An ultimate output of the quadratic filter is expressed by a sum by an adder 26 of the outputs of the respective FIR filters FIR0 to FIR5.

[0070]

Here, multiplication by 2 by the multipliers $13_2, \dots, 13_6$ may be treated as being equivalent to 1-bit left shift in the calculations employing binary numbers in a digital circuit, so that it is unnecessary to provide dedicated multipliers. Consequently, as multipliers for the quadratic filters for $M_2=6$, only the multipliers $12_1, \dots, 12_6, 19_1, \dots, 19_6, 20_1, \dots, 20_5, 21_1, \dots, 21_4, 22_1, \dots, 22_3, 23_1, 23_2$ and 24_1 , totaling at 27, are needed.

[0071]

The numbers of the multipliers for the quadratic filter of the second-order Volterra filter, shown in the equation (13), are shown in Fig.10 and in the following Table 2 for various values of M_2 . It should be noted that, for comparison with the number of the multipliers for the conventional case, Fig.10 and Table 2 also show the number of the multipliers of the quadratic filter of the conventional second-order Volterra filter as indicated by the equations (4) and (5).

[0072]

[Table 2]

M2	Number of multipliers of quadratic term of equation (4)	Number of multipliers of quadratic term of equation (5)	Number of multipliers of quadratic term of equation (13)
1	2	2	2
2	8	6	4
3	18	12	6
4	32	20	8
5	50	30	10
6	72	42	12
7	98	56	14
8	128	72	16
9	162	90	18
10	200	110	20
11	242	132	22
12	288	156	24
13	338	182	26
14	392	210	28
15	450	240	30

[0073]

As may be seen from Fig. 10 and Table 2, it is possible, according to the technique of this embodiment, to reduce the multiplication operations considerably, as compared to the case shown by the equation (4), by employing the conventional technique of reducing the calculations of the equation (5) simultaneously. Additionally, according to the technique of this embodiment, the multiplication operations may be reduced considerably as compared to a case where

the conventional technique for reducing calculation operations, shown in the equation (5), is used alone. The effect achieved is outstanding for a larger value of M_2 .

[0074]

It should be noted that in the above-described signal processing apparatus 10, the configuration as shown in Fig.9 is used for outputting respective elements of the two-dimensional array shown in Fig.8. However, since the configurations of the FRI filters are independent of one another, the number of the multipliers $19_1, \dots, 19_6, 20_1, \dots, 20_5, 21_1, \dots, 21_4, 22_1, \dots, 22_3, 23_1, 23_2$ and 24_1 , that is, the tap lengths of the respective FIR filters (FIR0 to FIR5), may be changed as long as performance necessary as a storage apparatus is sufficiently obtained as in a case where the equalization performance of the filters may be desired performance, for example, in a case where the data error rate exceeds a preset value, and the like. In similar manner, in a case where the filter equalization performance is sufficiently obtained with respect to desired performance, it is also possible to change the number of the FIR filters. However, the depth along the time axis proceeding from the diagonal term (FIR0) of the FIR filters (FIR0 to FIR5) towards the non-diagonal terms (FIR1 to FIR5) is thought to be a quantity relevant to the length of the inter-symbol interference (ISI) of PR (Partial Response) to be equalized, and hence the number of the FIR filters to be provided is desirably equal to or larger than the ISI length. Here, this length of the ISI of PR is e.g. 3 for PR (111). In a case where the tap coefficient is to be updated by an optional adaptive equalization algorithm, it is also possible to adopt a structure in which multipliers $13_2, \dots, 13_6$ for 1-bit shift are omitted. However, the configuration including the multipliers $13_2, \dots, 13_6$ is desirable in consideration of the delay otherwise caused in the convergence of the tap coefficients of

the quadratic filter. It is noted that, with the circuit configuration shown in Figs.11 and 12, it is also possible to prevent deterioration of the performance even in a case of reducing the number of the multipliers responsible for 1-bit shift or of omitting these multipliers from the circuit virtually.

[0075]

With the circuit configuration of the signal processing apparatus 10 shown in Fig.11, the circuit configuration shown in Fig.9 is further simplified from the circuit configuration of Fig.9, while the volume of calculations is further reduced as compared to that with Fig.9. More specifically, after the outputs FIR1 to FIR5 are summed together by the adder 27, the calculations corresponding to the multipliers $13_2, \dots, 13_6$ of Fig. 9 are carried out by a multiplier 28, an output of which is summed by an adder 29 to the output of the adder 25₁, whereby the width of bits needed in the filters FIR1 to FIR5 may be reduced, whilst the 1-bit shift operations for doubling calculations is reduced to one operation.

[0076]

The coefficients for doubling, represented by this 1-bit shift calculation operation, may be incorporated into no other than the tap coefficients, by doubling the respective tap coefficients from the outset. In a case of updating the tap coefficients using an adaptive equalization algorithm, doubling coefficients may be incorporated into no other than the tap coefficients or into a step gain parameter for updating the coefficients. In the latter case, if, with the step gain parameter of the diagonal term of μ_2 , the step gain parameter of the non-diagonal term is $2 \times \mu_2$, the doubling coefficients are unneeded in the respective FIR filters (FIR1 to FIR5), with the result that the multipliers $13_2, \dots, 13_6$ of Fig.9 are unnecessary, thus further simplifying the circuit configuration. Fig.12 shows the circuit configuration for such

case. In this case, the speed of updating the tap coefficients of the non-diagonal term is increased by a factor of two, which is equivalent to doubling the values of the tap coefficients of the non-diagonal terms.

[0077]

As described above, according to the signal processing apparatus 10 in this embodiment, the multiplication operations in non-linear equalization of an input signal having non-linear distortion may considerably be reduced, with the result that the circuit scale in implementation by LSI (Large-Scale Integrated Circuit) may be reduced. In addition, the volume of calculations in implementation by a DSP (Digital Signal Processor) and software may be diminished.

[0078]

Fig.13 shows an example of a circuit configuration of a linear filter for a case of $M_1 = 10$. The linear filter is made up by delay circuits $30_1, \dots, 30_9$, configured to delay the input signal $x(k)$, multipliers $31_1, \dots, 31_{10}$, configured to multiply the input signal $x(k)$ and delayed signals $x(k-1), \dots, x(k-9)$, output from the delay circuits $30_1, \dots, 30_9$, respectively, with preset filter coefficients, and an adder 32 for summing the outputs of the $31_1, \dots, 31_{10}$. The tap coefficients $h^{(1)}(i)$ ($i = 0, \dots, 9$) may be fixed tap coefficients or updated by any adaptive equalization algorithm.

[0079]

The configuration and the operation of a signal decoding apparatus of this embodiment, including the above-described signal processing apparatus 10 as a non-linear adaptive equalizer filter, will now be explained.

[0080]

For reproducing signals recorded on an optical disc 40, in a signal decoding apparatus 50 shown in Fig.14, the laser light from a laser light source, provided in an optical head 51, is irradiated

via an optical system on the optical disc 40, and return light therefrom is received by a light receiving device via an optical system provided in the optical head 51, so as to be subjected to photoelectric conversion. A signal from a light receiving device within the optical head 51 is amplified by an RF (Radio Frequency) amplifier 52 and quantized by an A/D (Analog/Digital) converter 53.

[0081]

The quantized signal is sent to a DPLL (Digital Phase Locked Loop) circuit 54, which then outputs RF signals equivalent to those sampled with clocks synchronized by the DPLL. The output signal from the DPLL circuit 54 is subjected to adaptive equalizing processing by a linear adaptive equalizing filter 55 and a non-linear adaptive equalizing filter 56, output signals from which are summed together by an adder 57. A sum signal $y(k)$ is sent to an LMS (Least Mean Square) error detection unit 58 and to a viterbi detection circuit 59. Meanwhile, the linear adaptive equalizing filter 55 performs calculations for the linear filter of the second-order Volterra filter indicated by the equation (13). On the other hand, the non-linear adaptive equalizing filter 56 performs calculations for the quadratic filter, and is configured as shown for example in Fig.9.

[0082]

When the signal from the adder 57 is sent to the LMS error detection unit 58, an error signal between the signal and a target detection value conforming to a preset equalization system is detected and, based on the thus-detected error signal, the tap coefficients of the linear filter and the quadratic filter are updated. The method for detecting an input code string within the LMS error detection unit 58 is arbitrary, and for example, the original code string is detected by a customary technique such

as threshold value detection, FDTS (Fixed Delay Tree Search), or viterbi detection unit. Specifically, the LMS error detection unit 58 convolves the code string that has been determined by the detection unit, with the PR coefficients desired to be equalized, to generate a provisional decision PR signal $d(k)$, and to detect an error signal $e(k)$ ($= d(k) - y(k)$) between the target provisional decision PR signal detection value $d(k)$ at a given time point k and the signal $y(k)$ from the adder 57 at a given time point k . Then, the tap coefficient $h^{(1)}(k+1:i)$ at the next time point of the linear filter, that is, at a time point $k+1$, is updated in accordance with the following equation (17):

[0083]

[Equation 13]

$$h^{(1)}(k+1:i) = h^{(1)}(k:i) + \mu_1 \cdot e(k) \cdot x(k-i) \quad \dots (17)$$

whilst the tap coefficient $h^{(2)}(k+1: i_1, i_2)$ at a time point $k+1$ of the quadratic filter is updated in accordance with the following equation (18):

$$h^{(2)}(k+1:i_1, i_2) = h^{(2)}(k:i_1, i_2) + \mu_2 \cdot e(k) \cdot x(k-i_1) \cdot x(k-i_2) \quad \dots (18)$$

In these equations (17) and (18), μ_1 and μ_2 denote step gain parameters of the LMS algorithm. The updated tap coefficients are sent to the linear adaptive equalizing filter 55 and to the non-linear adaptive equalizing filter 56.

[0084]

Further, the signal from the adder 57 is decoded based on the viterbi algorithm by a viterbi decoding circuit 59 and processed by a demodulating circuit 60 with demodulation which is the reverse

of the modulation used in recording. The replay data, resulting from demodulation, is sent to an error detection circuit 61 for error correction.

[0085]

Here, the concrete results of signal equalization are shown in Figs.15 and 16. Fig.15 shows an instance where equalization has been executed solely by the linear adaptive equalizing filter 55, and Fig.16 shows an instance where equalization has been executed by both the linear adaptive equalizing filter 55 and the non-linear adaptive equalizing filter 56. Meanwhile, in both of these instances, the system for equalization used is PR(111). In this embodiment, optical disc replay signals are generated by numerical value calculation simulation on a computer, in the signal decoding apparatus 50 of Fig.14, and sampled by a program equivalent to an A/D converter. A digital section of Fig.14 is structured by a signal processing program. A 15% asymmetry is produced in a simulation waveform.

[0086]

Eye patterns, obtained on interpolating pre-equalization digital data that is output from the DPLL circuit 54 of Fig.14 and digital data that is obtained on linear/ non-linear adaptive equalizing the output of the adder 57, with a SINC function serving as an interpolation function satisfying the sampling theorem for digital signal processing, will now be shown.

[0087]

In a case where only the linear adaptive equalizing filter 55 is used, non-linear characteristics generated in the pre-equalization waveform, that is, 15% asymmetry, are left over as non-linear equalization error even after equalization, and the lower eyes remain collapsed, as may be apparent on comparison of the output of the DPLL circuit 54 shown in Fig. 15(A), that is,

the pre-equalization eye pattern, to the post-equalization eye pattern shown in Fig. 15(B). On the other hand, with use of both the linear adaptive equalizing filter 55 and the non-linear adaptive equalizing filter 56, the non-linear characteristics, produced in the pre-equalization waveform, that is, the 15% asymmetry, are improved by the efficacy of the non-linear adaptive equalization filter, and eye patterns symmetrical in the up-and-down direction are produced, as may be apparent from comparison of the output of the DPLL circuit 54, that is, the pre-equalization eye pattern shown in Fig. 16(A), to the post-equalization eye pattern shown in Fig. 16(B).

[0088]

As described above, according to the signal decoding apparatus 50 of this invention, the non-linear distortion may effectively be corrected in reproducing signals recorded on the optical disc 40, by providing the non-linear adaptive equalizing filter 56 that is equivalent to the above-described signal processing apparatus 10, in addition to the linear adaptive equalizing filter 55 configured to perform the conventional linear adaptive equalization. In particular, this non-linear adaptive equalizing filter 56 is implemented easily because the volume of the multiplication operations needed may be considerably reduced more than conventionally.

[Brief Description of the Drawings]

[0089]

[Fig. 1] A conceptual diagram showing a two-dimensional array $x^{(2)}(k, i_1, i_2)$ in a case of $M_2 = 6$.

[Fig. 2] A conceptual diagram showing a two-dimensional array $h^{(2)}(i_1, i_2)$ in the case of $M_2 = 6$.

[Fig. 3] A diagram showing elements of a diagonal term $x^{(2)}(k, i, i)$ in the two-dimensional array shown in Fig.1.

[Fig. 4] A diagram showing elements of a non-diagonal term $x^{(2)}(k, i_1, i_2)$ in the two-dimensional array shown in Fig.1.

[Fig. 5] A conceptual view showing a two-dimensional array $W^{(2)}(k, i_1, i_2)$ in the case of $M_2 = 6$.

[Fig. 6] A diagram representing contents of respective elements of the two-dimensional array $W^{(2)}(k, i_1, i_2)$ shown in Fig.5, using $x^{(2)}(k, i_1, i_2)$.

[Fig. 7] A diagram showing the contents of the respective elements of the two-dimensional array $W^{(2)}(k, i_1, i_2)$, shown in Fig.5, as converted using the equation (12).

[Fig. 8] A diagram showing the contents of the respective elements of the two-dimensional array $W^{(2)}(k, i_1, i_2)$, shown in Fig.7, using $x^{(2)}(k, i_1, i_2)$.

[Fig. 9] A diagram illustrating an instance of a schematic structure of a signal processing apparatus in this embodiment.

[Fig. 10] A diagram illustrating another instance of a schematic structure of a signal processing apparatus in this embodiment.

[Fig. 11] A diagram illustrating yet another instance of a schematic structure of a signal processing apparatus in this embodiment.

[Fig. 12] A diagram showing a relation between a tap length of a quadratic filter of a second-order Volterra filter in this embodiment and the number of multipliers needed at that time.

[Fig. 13] A diagram showing an instance of a circuit structure of a linear filter in a case of $M_1 = 10$.

[Fig. 14] A diagram illustrating a schematic structure of a signal decoding apparatus in this embodiment.

[Figs. 15] Diagrams showing eye patterns in a case where an input signal exhibiting non-linear distortion is equalized only with a linear adaptive equalizing filter.

[Figs. 16] Diagram showing eye patterns in a case where an

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input signal exhibiting non-linear distortion is equalized with a linear adaptive equalizing filter and a non-linear adaptive equalizing filter.

[Fig. 17] A diagram showing a relation between a tap length of a quadratic filter of a conventional second-order Volterra filter and the number of multipliers needed at that time.

[Description of Reference Numerals]

[0090]

10 signal processing apparatus, 11₂, ..., 11₆ delay circuit, 12₁, ..., 12₆ multiplier, 13₂, ..., 13₆ multiplier, 14₁, ..., 14₅ delay circuit, 15₁, ..., 15₄ delay circuit, 16₁, ..., 16₃ delay circuit, 17₁, 17₂ delay circuit, 18₁ delay circuit, 19₁, ..., 19₆ multiplier, 20₁, ..., 20₅ multiplier, 21₁, ..., 24₄ multiplier, 22₁, ..., 22₃ multiplier, 23₁, 23₂ multiplier, 24₁ multiplier, 25₁, ..., 25₅ adder, 26 adder, 40 optical disc, 50 signal decoding apparatus, 51 optical head, 52 RF amplifier, 53 A/D converter, 54 DPLL circuit, 55 linear adaptive equalizing filter, 56 non-linear adaptive equalizing filter, 57 adder, 58 LMS error detection unit, 59 viterbi detection circuit, 60 demodulating circuit, 61 error correction circuit

【書類名】図面

【図 1】

i_1	i_2					
	0	1	2	3	4	5
0	$x^{(2)}(k,0,0)$	$x^{(2)}(k,0,1)$	$x^{(2)}(k,0,2)$	$x^{(2)}(k,0,3)$	$x^{(2)}(k,0,4)$	$x^{(2)}(k,0,5)$
1	$x^{(2)}(k,1,0)$	$x^{(2)}(k,1,1)$	$x^{(2)}(k,1,2)$	$x^{(2)}(k,1,3)$	$x^{(2)}(k,1,4)$	$x^{(2)}(k,1,5)$
2	$x^{(2)}(k,2,0)$	$x^{(2)}(k,2,1)$	$x^{(2)}(k,2,2)$	$x^{(2)}(k,2,3)$	$x^{(2)}(k,2,4)$	$x^{(2)}(k,2,5)$
3	$x^{(2)}(k,3,0)$	$x^{(2)}(k,3,1)$	$x^{(2)}(k,3,2)$	$x^{(2)}(k,3,3)$	$x^{(2)}(k,3,4)$	$x^{(2)}(k,3,5)$
4	$x^{(2)}(k,4,0)$	$x^{(2)}(k,4,1)$	$x^{(2)}(k,4,2)$	$x^{(2)}(k,4,3)$	$x^{(2)}(k,4,4)$	$x^{(2)}(k,4,5)$
5	$x^{(2)}(k,5,0)$	$x^{(2)}(k,5,1)$	$x^{(2)}(k,5,2)$	$x^{(2)}(k,5,3)$	$x^{(2)}(k,5,4)$	$x^{(2)}(k,5,5)$

【図2】

i_1	i_2	0	1	2	3	4	5
0	$h^{(2)}(0,0)$	$h^{(2)}(0,1)$	$h^{(2)}(0,2)$	$h^{(2)}(0,3)$	$h^{(2)}(0,4)$	$h^{(2)}(0,5)$	
1	$h^{(2)}(1,0)$	$h^{(2)}(1,1)$	$h^{(2)}(1,2)$	$h^{(2)}(1,3)$	$h^{(2)}(1,4)$	$h^{(2)}(1,5)$	
2	$h^{(2)}(2,0)$	$h^{(2)}(2,1)$	$h^{(2)}(2,2)$	$h^{(2)}(2,3)$	$h^{(2)}(2,4)$	$h^{(2)}(2,5)$	
3	$h^{(2)}(3,0)$	$h^{(2)}(3,1)$	$h^{(2)}(3,2)$	$h^{(2)}(3,3)$	$h^{(2)}(3,4)$	$h^{(2)}(3,5)$	
4	$h^{(2)}(4,0)$	$h^{(2)}(4,1)$	$h^{(2)}(4,2)$	$h^{(2)}(4,3)$	$h^{(2)}(4,4)$	$h^{(2)}(4,5)$	
5	$h^{(2)}(5,0)$	$h^{(2)}(5,1)$	$h^{(2)}(5,2)$	$h^{(2)}(5,3)$	$h^{(2)}(5,4)$	$h^{(2)}(5,5)$	

【図3】

i_1	i_2	0	1	2	3	4	5
0		$x^{(2)}(k,0,0)$					
1			$x^{(2)}(k,1,1)$				
2				$x^{(2)}(k,2,2)$			
3					$x^{(2)}(k,3,3)$		
4						$x^{(2)}(k,4,4)$	
5							$x^{(2)}(k,5,5)$

【図4】

i_2	0	1	2	3	4	5
i_1	0	$x^{(2)}(k,0,1)$	$x^{(2)}(k,0,2)$	$x^{(2)}(k,0,3)$	$x^{(2)}(k,0,4)$	$x^{(2)}(k,0,5)$
1			$x^{(2)}(k,1,2)$	$x^{(2)}(k,1,3)$	$x^{(2)}(k,1,4)$	$x^{(2)}(k,1,5)$
2				$x^{(2)}(k,2,3)$	$x^{(2)}(k,2,4)$	$x^{(2)}(k,2,5)$
3					$x^{(2)}(k,3,4)$	$x^{(2)}(k,3,5)$
4						$x^{(2)}(k,4,5)$
5						

【図5】

i_1	i_2	0	1	2	3	4	5
0	0	$W^{(2)}(k,0,0)$	$W^{(2)}(k,0,1)$	$W^{(2)}(k,0,2)$	$W^{(2)}(k,0,3)$	$W^{(2)}(k,0,4)$	$W^{(2)}(k,0,5)$
1	0	0	$W^{(2)}(k,1,1)$	$W^{(2)}(k,1,2)$	$W^{(2)}(k,1,3)$	$W^{(2)}(k,1,4)$	$W^{(2)}(k,1,5)$
2	0	0	0	$W^{(2)}(k,2,2)$	$W^{(2)}(k,2,3)$	$W^{(2)}(k,2,4)$	$W^{(2)}(k,2,5)$
3	0	0	0	0	$W^{(2)}(k,3,3)$	$W^{(2)}(k,3,4)$	$W^{(2)}(k,3,5)$
4	0	0	0	0	0	$W^{(2)}(k,4,4)$	$W^{(2)}(k,4,5)$
5	0	0	0	0	0	0	$W^{(2)}(k,5,5)$

【図 6】

i_1	i_2	0	1	2	3	4	5
0	$x^{(2)}(k,0,0)$	$2x^{(2)}(k,0,1)$	$2x^{(2)}(k,0,2)$	$2x^{(2)}(k,0,3)$	$2x^{(2)}(k,0,4)$	$2x^{(2)}(k,0,5)$	
1	0	$x^{(2)}(k,1,1)$	$2x^{(2)}(k,1,2)$	$2x^{(2)}(k,1,3)$	$2x^{(2)}(k,1,4)$	$2x^{(2)}(k,1,5)$	
2	0	0	$x^{(2)}(k,2,2)$	$2x^{(2)}(k,2,3)$	$2x^{(2)}(k,2,4)$	$2x^{(2)}(k,2,5)$	
3	0	0	0	$x^{(2)}(k,3,3)$	$2x^{(2)}(k,3,4)$	$2x^{(2)}(k,3,5)$	
4	0	0	0	0	$x^{(2)}(k,4,4)$	$2x^{(2)}(k,4,5)$	
5	0	0	0	0	0	$x^{(2)}(k,5,5)$	

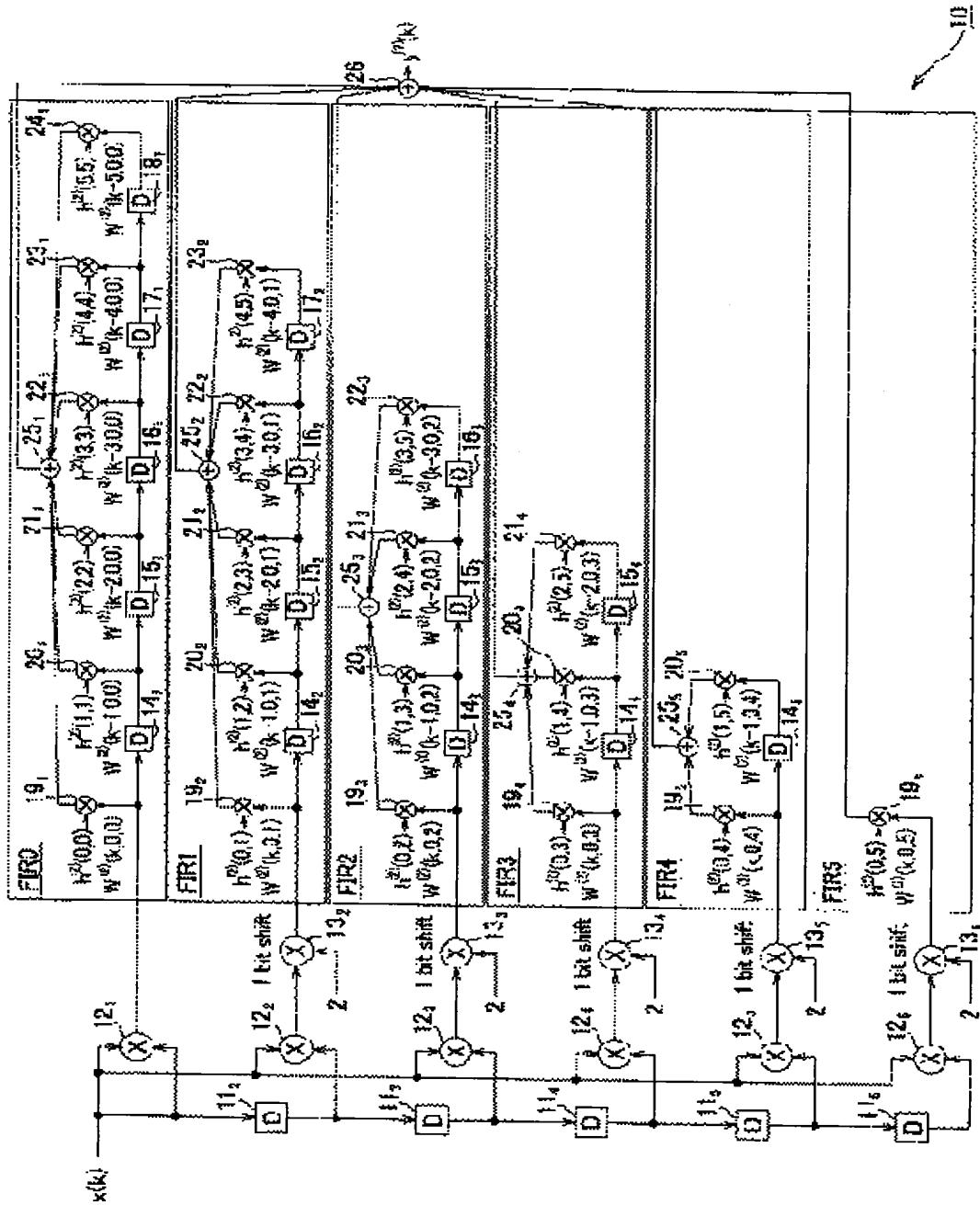
【図 7】

i_2	0	1	2	3	4	5
i_1	$W^{(2)}(k,0,0)$	$W^{(2)}(k,0,1)$	$W^{(2)}(k,0,2)$	$W^{(2)}(k,0,3)$	$W^{(2)}(k,0,4)$	$W^{(2)}(k,0,5)$
1	0	$W^{(2)}(k-1,0,0)$	$W^{(2)}(k-1,0,1)$	$W^{(2)}(k-1,0,2)$	$W^{(2)}(k-1,0,3)$	$W^{(2)}(k-1,0,4)$
2	0	0	$W^{(2)}(k-2,0,0)$	$W^{(2)}(k-2,0,1)$	$W^{(2)}(k-2,0,2)$	$W^{(2)}(k-2,0,3)$
3	0	0	0	$W^{(2)}(k-3,0,0)$	$W^{(2)}(k-3,0,1)$	$W^{(2)}(k-3,0,2)$
4	0	0	0	0	$W^{(2)}(k-4,0,0)$	$W^{(2)}(k-4,0,1)$
5	0	0	0	0	0	$W^{(2)}(k-5,0,0)$

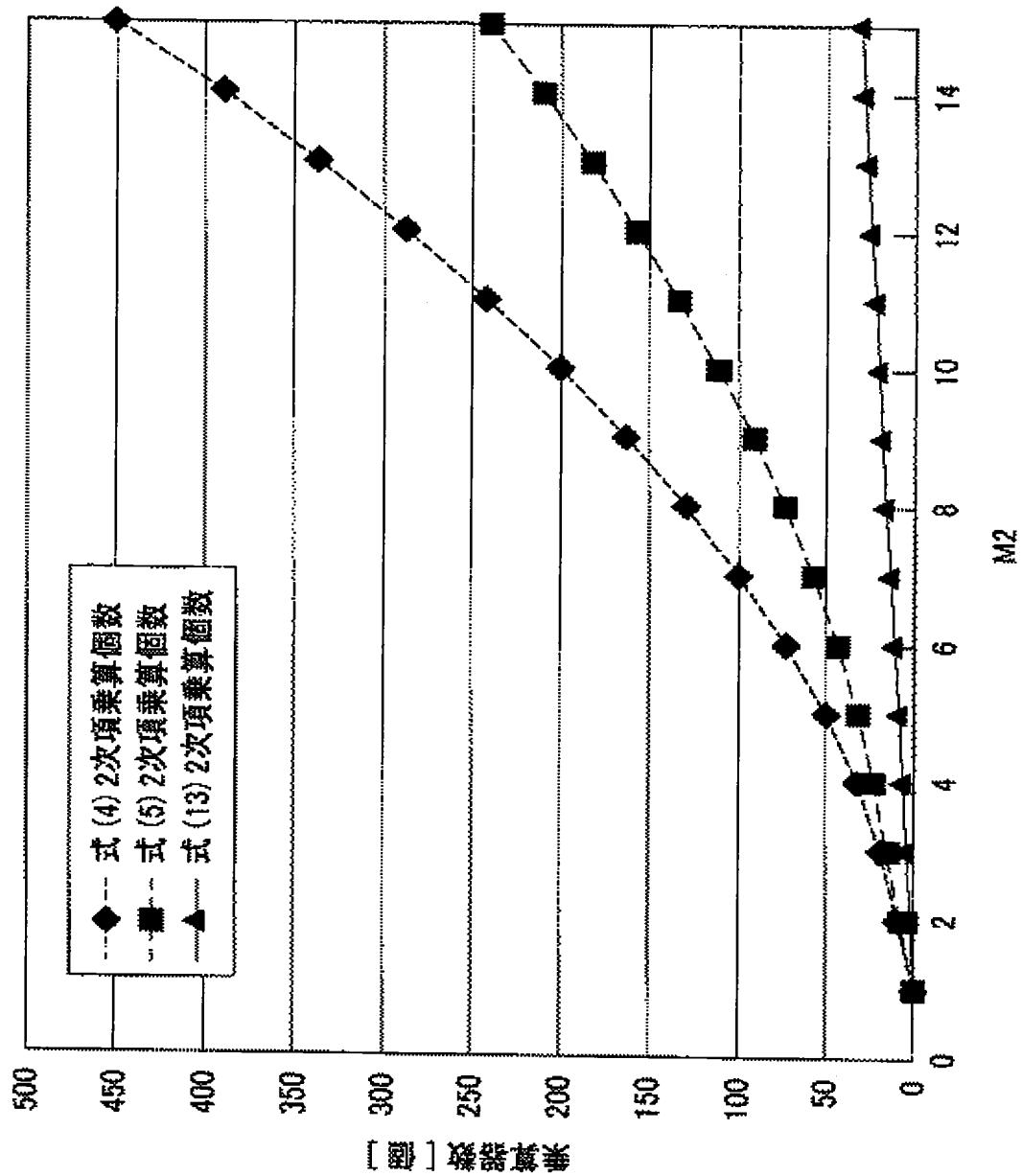
【図 8】

i_1	i_2	0	1	2	3	4	5
0	$x^{(2)}(k,0,0)$	$2x^{(2)}(k,0,1)$	$2x^{(2)}(k,0,2)$	$2x^{(2)}(k,0,3)$	$2x^{(2)}(k,0,4)$	$2x^{(2)}(k,0,5)$	
1	0	$x^{(2)}(k-1,0,0)$	$2x^{(2)}(k-1,0,1)$	$2x^{(2)}(k-1,0,2)$	$2x^{(2)}(k-1,0,3)$	$2x^{(2)}(k-1,0,4)$	
2	0	0	$x^{(2)}(k-2,0,0)$	$2x^{(2)}(k-2,0,1)$	$2x^{(2)}(k-2,0,2)$	$2x^{(2)}(k-2,0,3)$	
3	0	0	0	$x^{(2)}(k-3,0,0)$	$2x^{(2)}(k-3,0,1)$	$2x^{(2)}(k-3,0,2)$	
4	0	0	0	0	$x^{(2)}(k-4,0,0)$	$2x^{(2)}(k-4,0,1)$	
5	0	0	0	0	0	$x^{(2)}(k-5,0,0)$	

【図 9】

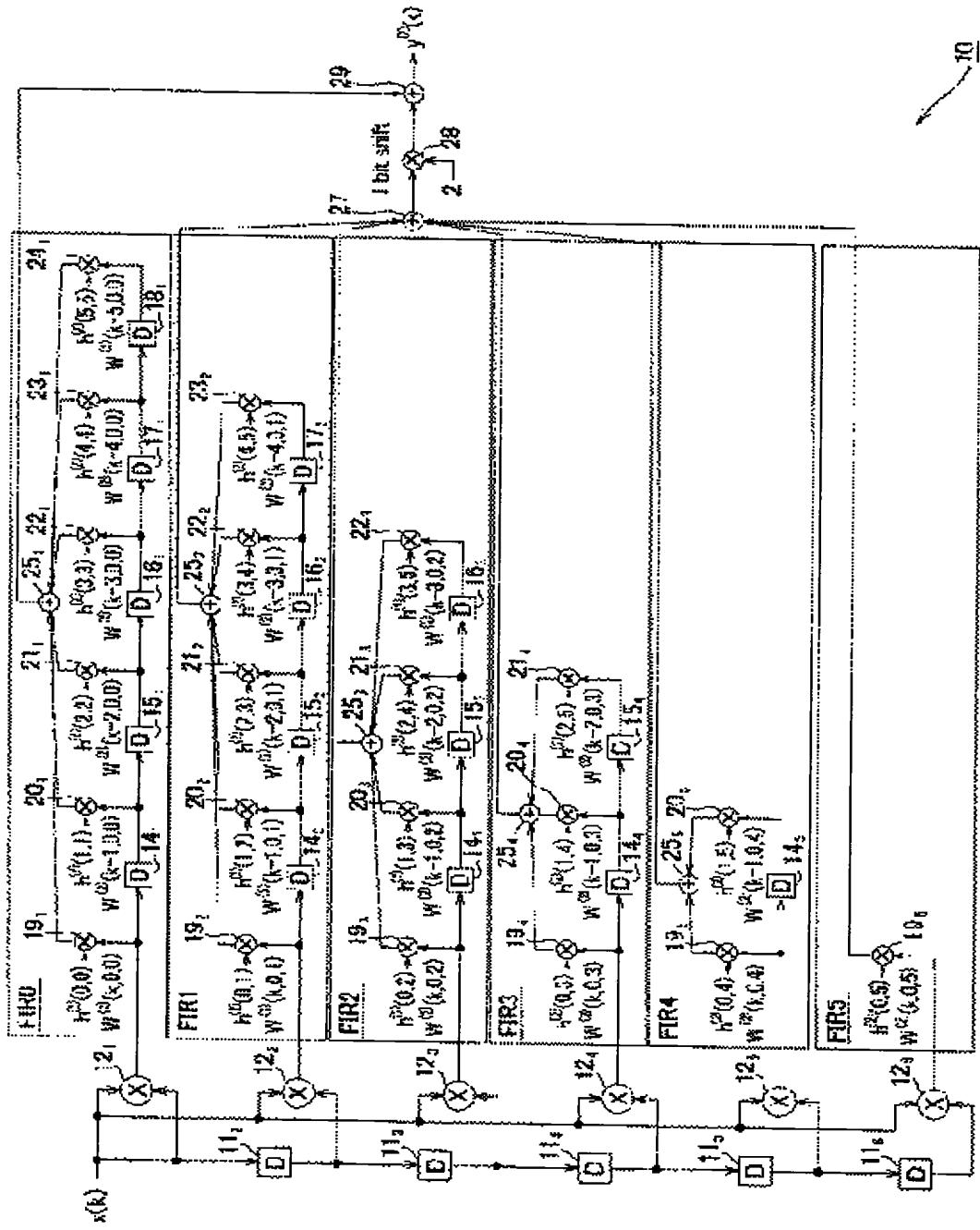


【図10】

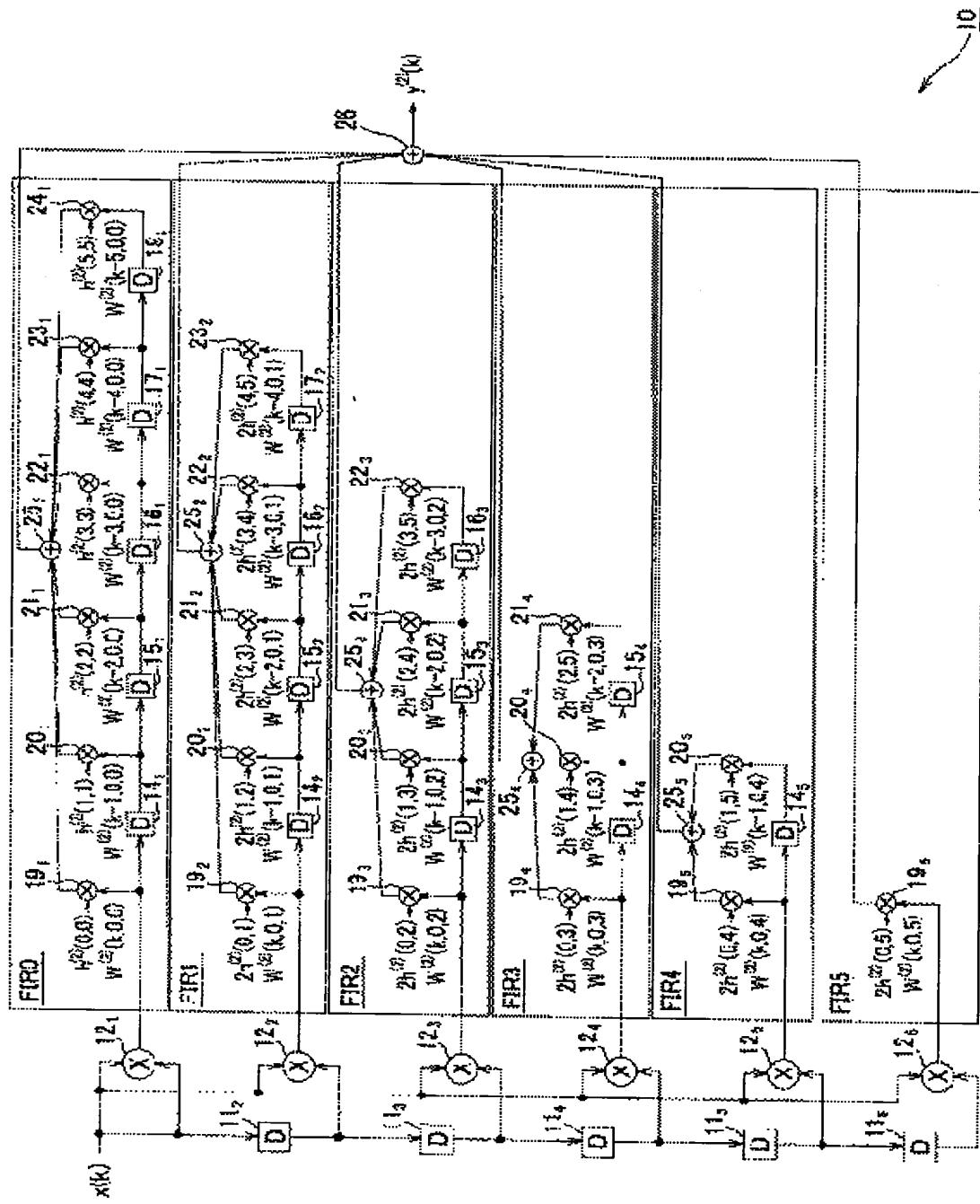


【図10】 繰繰計算

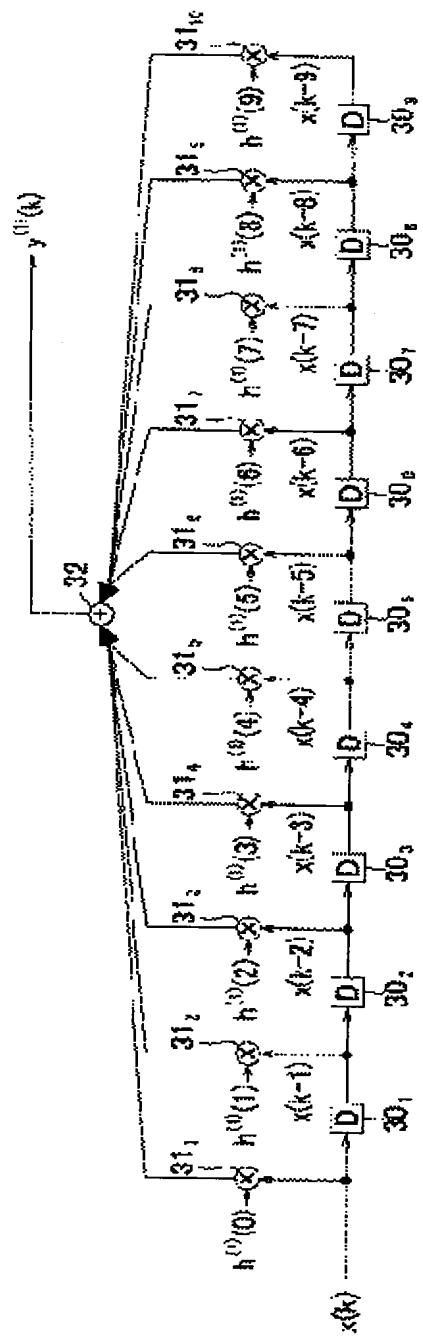
【図 1-1】



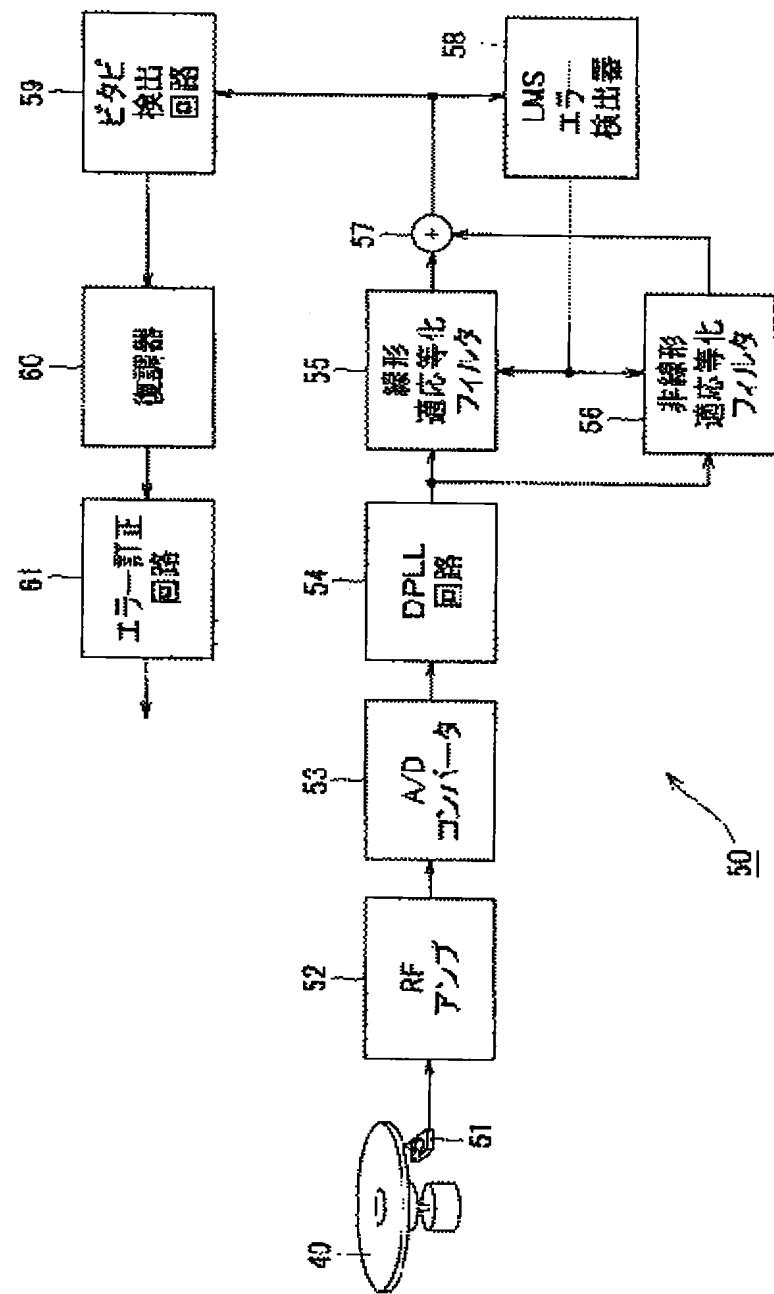
【図12】



【図 1 3】



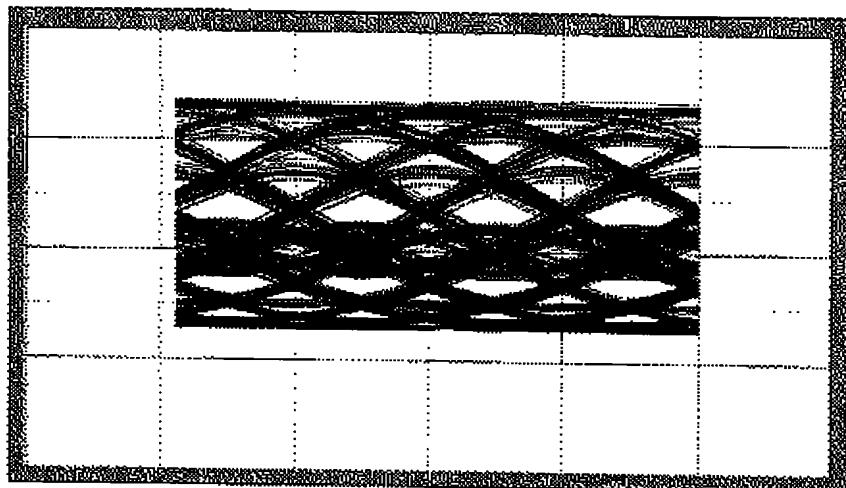
【図14】



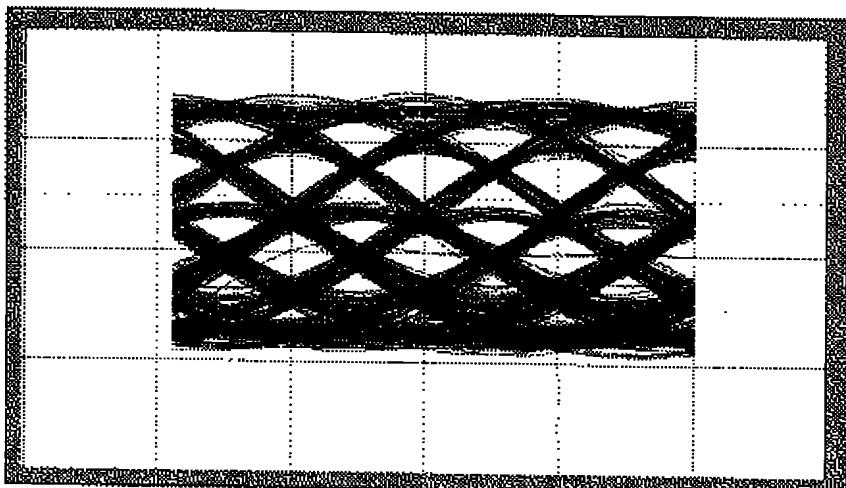
S05P0423US00

【図15】

(A)



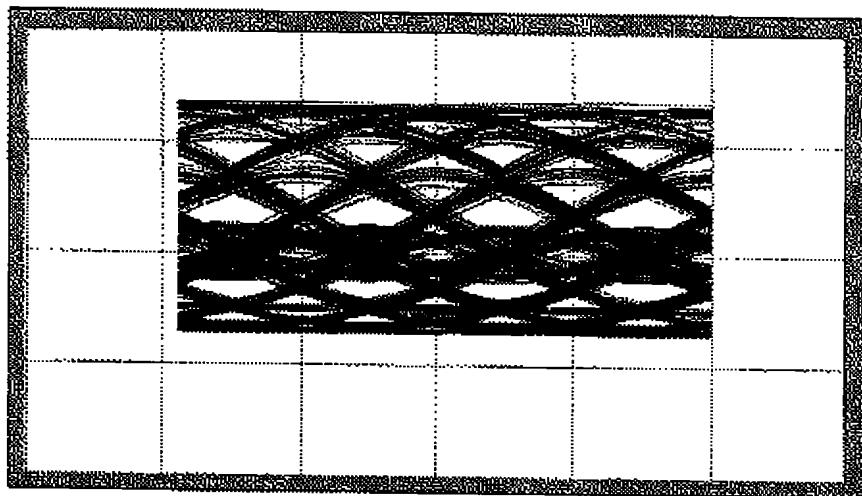
(B)



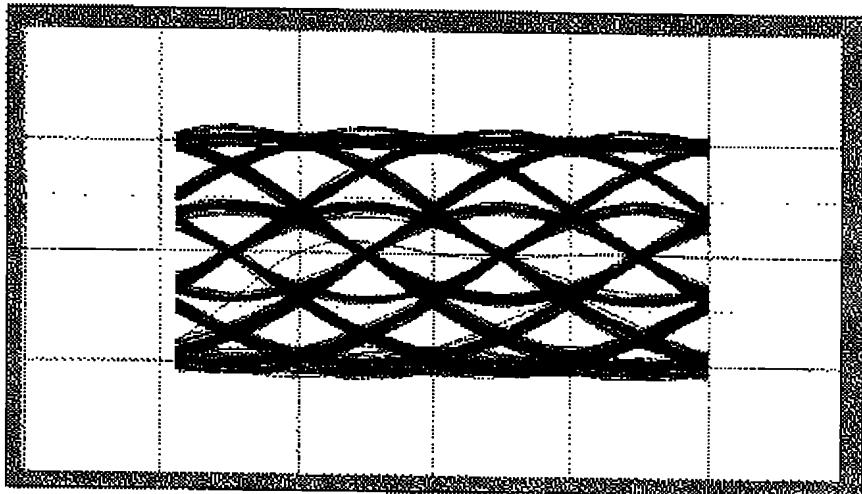
S05P0423US00

【図16】

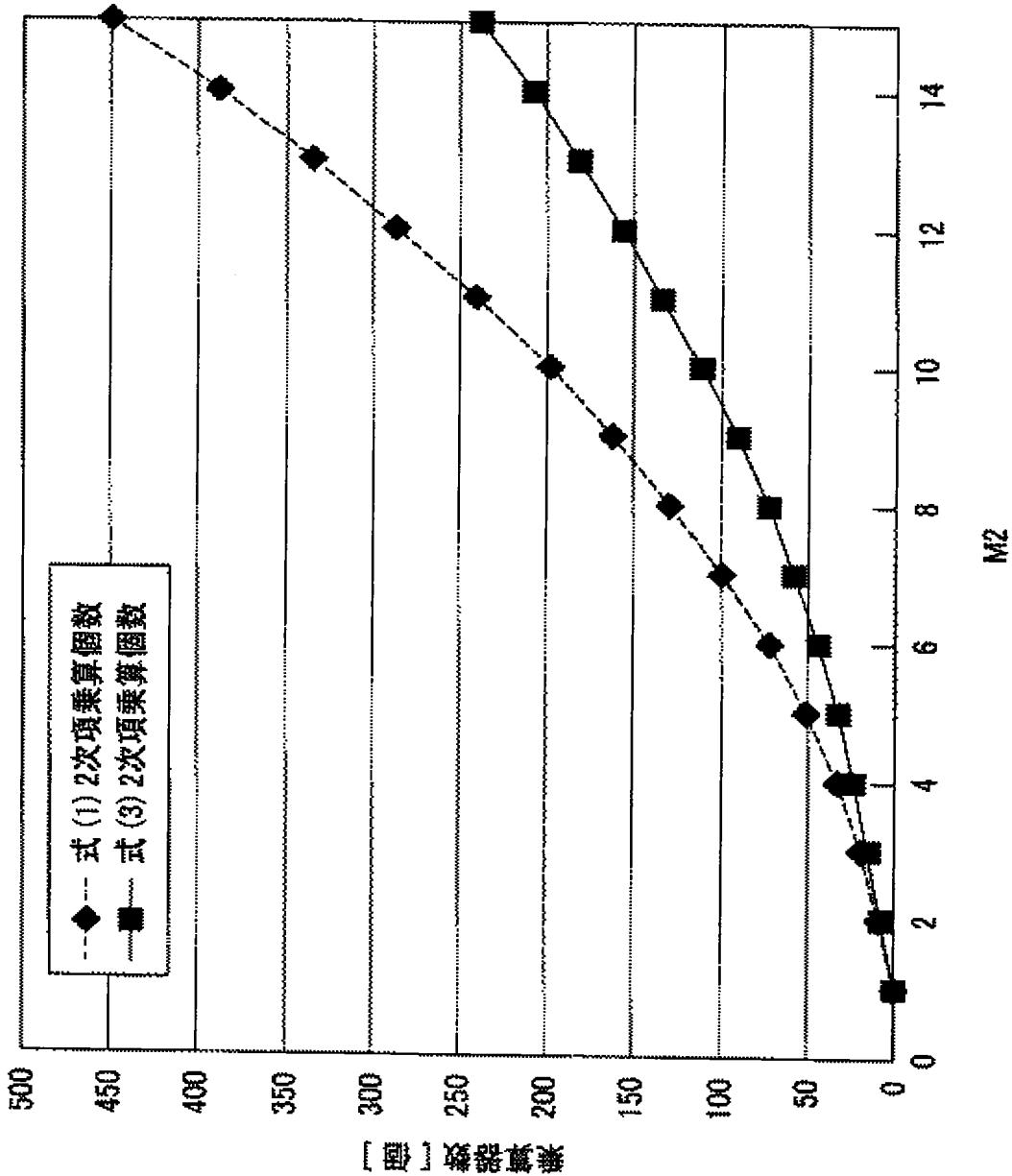
(A)



(B)



【図17】



【書類名】 図面 [Document Name] Drawings

【図 1】 [FIG. 1]

【図 2】 [FIG. 2]

【図 3】 [FIG. 3]

【図 4】 [FIG. 4]

【図 5】 [FIG. 5]

【図 6】 [FIG. 6]

【図 7】 [FIG. 7]

【図 8】 [FIG. 8]

【図 9】 [FIG. 9]

【図 10】 [FIG. 10]

乗算器数 (個)	NUMBER OF MULTIPLIERS (UNIT)
式 (4) 2 次項乗算個数 OF EQUATION (4)	NUMBER OF MULTIPLIERS OF QUADRATIC TERM
式 (5) 2 次項乗算個数 OF EQUATION (5)	NUMBER OF MULTIPLIERS OF QUADRATIC TERM
式 (13) 2 次項乗算個数 OF EQUATION (13)	NUMBER OF MULTIPLIERS OF QUADRATIC TERM

【図 1 1】 [FIG. 11]

【図 1 2】 [FIG. 12]

【図 1 3】 [FIG. 13]

【図 1 4】 [FIG. 14]

RF アンプ	RF AMPLIFIER
A/D コンバータ	A/D CONVERTER
DPLL 回路	DPLL CIRCUIT
線形適応等化フィルタ	LINEAR ADAPTIVE EQUALIZING FILTER
非線形適応等化フィルタ	NON-LINEAR ADAPTIVE EQUALIZING FILTER
LMS エラー検出器	LMS ERROR DETECTION UNIT
ビタビ検出回路	VITERBI DETECTION CIRCUIT
復調器	DEMODULATOR
エラー訂正回路	ERROR CORRECTION CIRCUIT

【図 1 5】 [FIGS. 15]

【図 1 6】 [FIGS. 16]

【図 1 7】 [FIG. 17]

乗算器数 (個)	NUMBER OF MULTIPLIERS (UNIT)
式 (1) 2 次項乗算個数 OF EQUATION (1)	NUMBER OF MULTIPLIERS OF QUADRATIC TERM
式 (3) 2 次項乗算個数	NUMBER OF MULTIPLIERS OF QUADRATIC TERM

S05P0423US00

OF EQUATION (3)

[Document Name] Abstract of the Disclosure

[Abstract]

[Object]

Multiplication operations in equalization of an input signal having non-linear distortion is considerably reduced.

[Means for Solving] A signal processing apparatus 10 that implements a quadratic term of a second-order Volterra filter includes multiplication means for multiplying a first input signal and a second input signal. Each of the multiplication means includes one or more series-connected delay means for delaying a signal output from the multiplication means, each by a unit time, and coefficient multiplying means for multiplying a signal output from each multiplication means and a signal output from each delay means, each by a preset coefficient. A number n , n being an integer not less than unity, of the multiplication means are connected in parallel with one another, and a k' th multiplication means, k being an integer such that $1 \leq k \leq n$, uses a signal delayed from the first signal a time equal to $(k-1)$ times by the unit time, as the second signal.

[Selected Drawing] Fig. 9